We claim

1. A memory module standardized and connectable to a computer body generating a predetermined number of address signals and a plurality of select signals representing a select or unselected state of each of memory spaces having a capacity corresponding to the predetermined of the address signals, the memory module comprising:

a memory receiving a memory select signal representing a select or unselected state and a plurality of address signals greater than the predetermined number of the address signals, and permitting data corresponding the plurality of the address signals to be accessible when the memory select signal represents a selected state; and

a memory circuit receiving the predetermined number of the address signals and a plurality of select signals from the computer body, generating the memory select signal and an additional address signal added to the predetermined number of the address according to the inputted select signals, and providing the generated memory select signal, the generated additional address signal, and the predetermined number of the inputted address signals to the memory to permit the computer body to access data corresponding thereto.

2. The memory module of claim 1, wherein the memory circuit makes the memory select signal represent a selected state of the memory when either of the plurality of the inputted select signals represents a selected state of the memory space, and makes the memory select signal represent an unselected state of the memory when all the plurality of the inputted select signals represent

an unselected state of the memory space.

3. The memory module of claim 1, wherein the computer body generates two types of select signals representing a selected or unselected state of two memory spaces of a capacity corresponding to the predetermined number of the address signals,

and wherein the memory circuit receives either of the two types of the select signals from the computer body, and provides the either of the select signals as the additional address to the memory.

4. The memory module of claim 1, wherein, when the memory receives a pulse-shaped clock signal and a memory clock enable signal representing a valid or invalid state of an input of the clock signal, and, the memory is operable according to the clock signal when the clock enable signal is valid;

wherein the computer body generates the clock signal and a plurality of clock enable signals representing a valid or invalid state of an input of the clock signal for each of the plurality of the memory spaces; and

wherein the memory circuit receives the clock signal and the plurality of the clock enable signals, generates the memory clock enable signal according to the plurality of the inputted clock enable signals, and provides the memory clock enable signal and the inputted clock signal to the memory.

5. The memory module of claim 1, wherein the memory circuit makes the memory clock enable signal represent a valid state of a clock signal input of the memory when any one of the inputted plurality of the clock enable signals represent a valid state

of a clock signal input of the memory, and makes the memory clock enable signal represent an invalid state of a clock signal input of the memory space when all the inputted plurality of the clock enable signals represent an invalid state of a clock signal input of the memory space.

6. The memory module of claim 1, wherein the additional address signal represents an address upper than one represented by the predetermined number of the address signals.

7. A memory module standardized and connectable to a computer body generating a predetermined number of address signals and a select signal representing a selected or unselected state of each of a plurality of memory spaces having a capacity corresponding to the predetermined number of the address signals, the memory module comprising:

a memory receiving a plurality of address signals greater than the predetermined number of the address signals and permitting data corresponding thereto to be accessible; and

a memory circuit receiving the predetermined number of the address signals and a select signal, generating an additional address added to the predetermined number of the address signals according to the inputted select signal, and, by providing the additional address signal and the predetermined number of the inputted address signals to the memory, permitting data corresponding thereto to be accessible by the computer body.

8. A memory-assist module wherein

when a memory connected to a computer body receives a memory select signal representing a select or unselected state and a

plurality of address signals greater than a predetermined number of address signals, and permits data corresponding to the plurality of the address signals to be accessible by the computer body when the memory select signal represents a selected state,

the computer body generating the predetermined number of the address signals and a plurality of select signals representing a select or unselected state of each of a plurality of memory spaces having a capacity corresponding to the predetermined number of the address signals,

the predetermined number of the address signals and the plurality of the select signals are inputted from the computer body, the memory select signal and an additional address signal added to the predetermined number of the address signals are generated according to the inputted select signals, and the generated memory select signal, the generated additional address signal, and the predetermined number of the inputted address signals are provided to the memory.

9. A memory-assist module wherein

when a memory connected to a computer body receives a plurality of address signals greater than a predetermined number of a address signals, and permits the corresponding data to be accessible by the computer body,

the computer body generating the predetermined number of the address signals and a select signal representing a select or unselected state of each of a plurality of memory spaces having a capacity corresponding to the predetermined number of the address signals,

the predetermined number of the address signals and a select signal are inputted from the computer body, an additional address signal added to the predetermined number of the address signals is generated according to the inputted select signal, and the additional address signal and the inputted predetermined number of the address signals are provided to the memory.